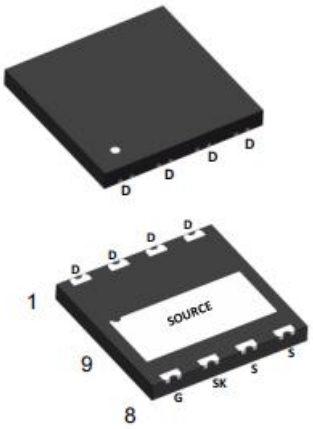
HGL70R190E-W

700V GaN Enhancement-mode Power Transistor

1. General description

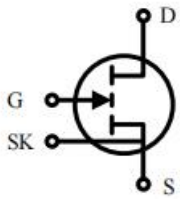
700V GaN-on-Silicon Enhancement-mode Power Transistor in package DFN8*8

2. Features



- Enhancement mode transistor-Normally off power switch
- Ultra high switching frequency
- No reverse-recovery charge
- Low gate charge, low output charge
- Qualified for industrial applications according to JEDEC Standards
- ESD safeguard
- RoHS, Pb-free, REACH-compliant

3. Applications



- AC-DC converters
- DC-DC converters
- Totem pole PFC
- Fast battery charging
- High density power conversion
- High efficiency power conversion

4. Key performance parameters

Table 1 Key performance parameters at T_j = 25 °C

Parameter	Value	Unit
$V_{DS,max}$	700	V
$R_{DS(on),max}$ @ V_{GS} = 6V	190	mΩ
$Q_{G,typ}$ @ V_{DS} = 400V	2.8	nC
$I_{D,pulse}$	20.5	A
Q_{OSS} @ V_{DS} = 400V	24.5	nC
Q_{rr} @ V_{DS} = 400V	0	nC

5. Pin information

Table 2 Pin information

Gate	Drain	Kelvin Source	Source
8	1,2,3,4	7	5,6,9

Table 3 Ordering information

Type/Ordering Code	Package	Product Code
HGL70R190E-W	DFN8*8	HGL70R190E-W

6. Maximum ratings

at T_j = 25 °C unless otherwise specified.
Exceeding the maximum ratings may destroy the device. For further information, contact Huake sales office.

Table 4 Maximum ratings

Parameter	Symbol	Values	Unit	Note/Test Condition
Drain source voltage	$V_{DS,max}$	700	V	V_{GS} = 0 V, T_j = -55 °C to 150 °C
Drain source voltage transient [1]	$V_{DS(transient)}$	800	V	V_{GS} = 0 V
Drain source voltage, pulsed [2]	$V_{DS,pulse}$	750	V	T_j =25 °C; total time<10h
Drain source voltage, pulsed [2]	$V_{DS,pulse}$	750	V	T_j =125 °C; total time<1h
Continuous current, drain source	I_D	11.5	A	T_c = 25 °C
Pulsed current, drain source [3]	$I_{D,pulse}$	20.5	A	T_c = 25 °C; V_G = 6 V; t_{PULSE}=10µs
Pulsed current, drain source [3]	$I_{D,pulse}$	11.5	A	T_c = 125 °C;V_G = 6 V; t_{PULSE}=10µs
Gate source voltage, continuous [4]	V_{GS}	-1.4 to +7	V	Tj = -55 °C to 150 °C
Gate source voltage, pulsed	$V_{GS,pulse}$	-20 to +10	V	Tj = -55 °C to 150 °C; t_{Pulse} = 50 ns, f = 100 kHz open drain
Power dissipation	P_{tot}	83	W	T_c = 25 °C
Operating temperature	T_j	-55 to +150	˚C	
Storage temperature	T_{stg}	-55 to +150	˚C	

1 $V_{DS(transient)}$ is intended for non-repetitive events, t_{PULSE} < 200 µs
2 $V_{DS,pulse}$ is intended for repetitive pulse, t_{PULSE} < 100 ns
3 Limit was extracted from characterization test, not measured during production
4 The minimum V_{GS} is clamped by ESD protection circuit, as shown in Figure 10

7. Thermal characteristics

Table 5 Thermal characteristics

Parameter	Symbol	Values	Unit	Note/Test Condition
Thermal resistance, junction-case	R_{thJC}	1.49	°C/W	
Maximum reflow soldering temperature	T_{sold}	260	°C	MSL3

8. Electric characteristics

at Tj = 25 °C, unless specified otherwise

Table 6 Static characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Gate threshold voltage	$V_{GS(th)}$	1.2	1.7	2.5	V	I_D=12.2mA; V_{DS}=V_{GS}; T_j=25 °C
		--	1.7	--		I_D=12.2mA; V_{DS}=V_{GS}; T_j =150 °C
Drain-source leakage current	I_{DSS}	--	0.45	20	μA	V_{DS}=700V; V_{GS}=0V; T_j =25°C
		--	6	--		V_{DS}=700V; V_{GS}=0V; T_j =150°C
Gate-source leakage current	I_{GSS}	--	60	--	μA	V_{GS}=6V; V_{DS}=0V
Drain-source on-state resistance	$R_{DS(on)}$	--	138	190	mΩ	V_{GS}=6V; I_D=3.9A; T_j=25 °C
		--	300	--		V_{GS}=6V; I_D=3.9A; T_j=150°C
Gate resistance	R_G	--	5.8	--	Ω	f =5MHz; open drain

Table 7 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	--	96	--	pF	V_{GS} =0V; V_{DS} =400V; f =100kHz
Output capacitance	C_{oss}	--	30	--	pF	V_{GS} =0V; V_{DS} =400V; f =100 kHz
Reverse transfer capacitance	C_{rss}	--	0.5	--	pF	V_{GS} =0V; V_{DS} =400V; f =100 kHz
Effective output capacitance, energy related [1]	$C_{o(er)}$	--	43	--	pF	V_{GS} =0V; V_{DS} = 0 to 400V
Effective output capacitance, time related [2]	$C_{o(tr)}$	--	60	--	pF	V_{GS} =0V; V_{DS} = 0 to 400V
Output charge	Q_{OSS}	--	24.5	--	nC	V_{GS} =0V; V_{DS} = 0 to 400V
Turn-on delay time	$t_{d(on)}$	--	1.4	--	ns	V_{DS} = 400V; I_D=8A; L = 318 μH; V_{GS} = 6V; R_{on} = 10 Ω; R_{off} = 2 Ω; See Figure 22
Turn-off delay time	$t_{d(off)}$	--	1.7	--	ns	
Rise time	t_r	--	4	--	ns	
Fall time	t_f	--	4	--	ns	

1 $C_{O(er)}$ is the fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 400 V

2 $C_{O(tr)}$ is the fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 400 V

Table 8 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Gate charge	Q_G	--	2.8	--	nC	V_{GS}= 0 to 6 V; V_{DS} = 400 V; I_D= 3.9 A
Gate-source charge	Q_{GS}	--	0.25	--	nC	
Gate-drain charge	Q_{GD}	--	1.1	--	nC	
Gate Plateau Voltage	V_{Plat}	--	2.2	--	V	V_{DS} = 400 V; I_D= 3.9 A

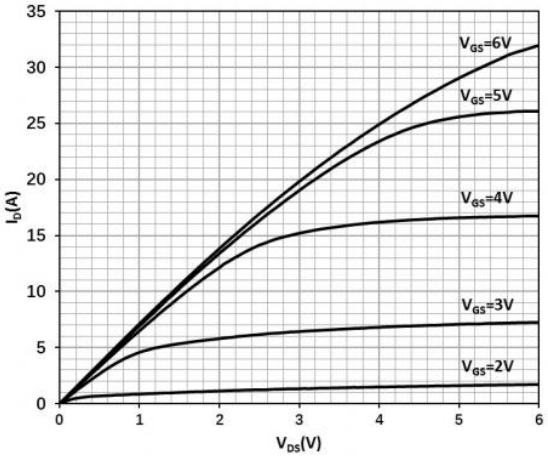
Table 9 Reverse conduction characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Source-Drain reverse voltage	V_{SD}	--	2.6	--	V	V_{GS} = 0 V; I_{SD}= 3.9 A
Pulsed current, reverse	$I_{S,pulse}$	--	--	20.5	A	V_{GS} = 6 V; t_{PULSE}=10µs
Reverse recovery charge	Q_{rr}	--	0	--	nC	I_{SD} =3.9 A; V_{DS} = 400 V
Reverse recovery time	t_{rr}	--	0	--	ns	
Peak reverse recovery current	I_{rrm}	--	0	--	A	

9. Electric characteristics diagrams

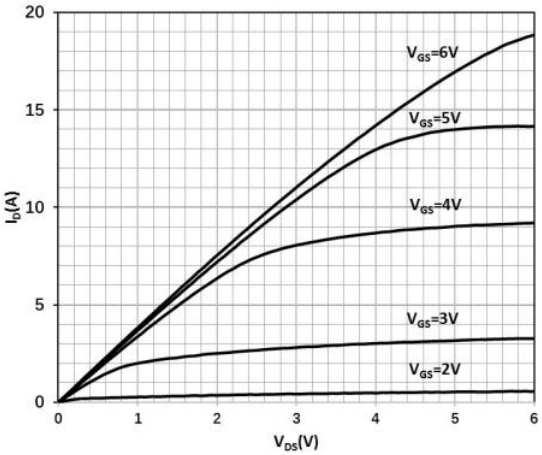
at Tj = 25 °C, unless specified otherwise

Figure 1 Typ. output characteristics



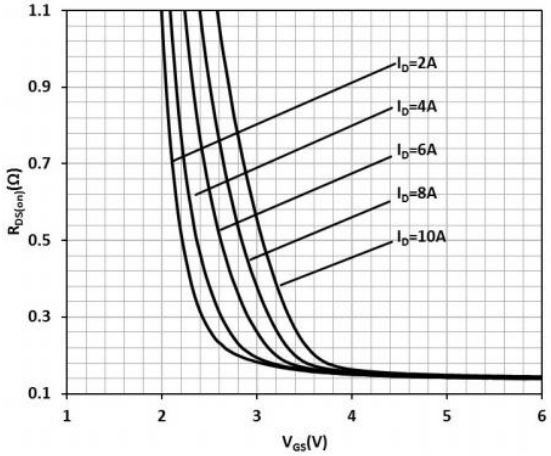
$I_D = f(V_{DS},V_{GS})$; T_j = 25 °C

Figure 2 Typ. output characteristics



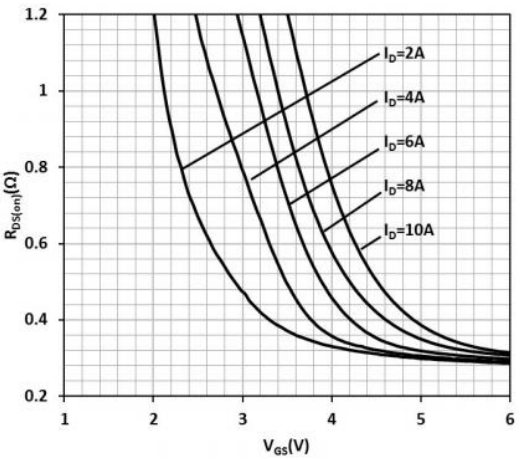
$I_D = f(V_{DS},V_{GS})$; T_j = 125 °C

Figure 3 Typ. Drain-source on-state resistance



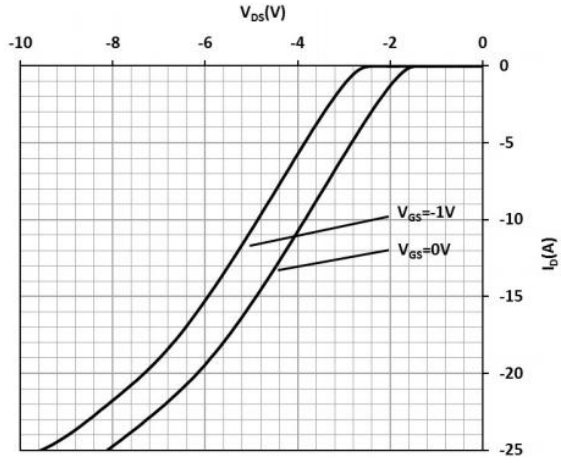
$R_{DS(on)} = f(I_{DS},V_{GS})$; T_j = 25 °C

Figure 4 Typ. Drain-source on-state resistance



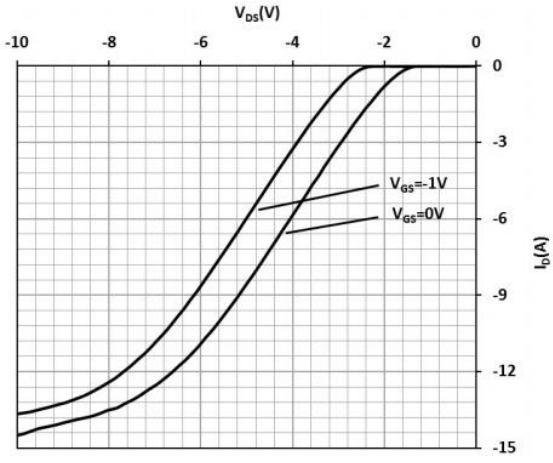
$R_{DS(on)} = f(I_{DS},V_{GS})$; T_j = 125 °C

Figure 5 Typ. channel reverse characteristics



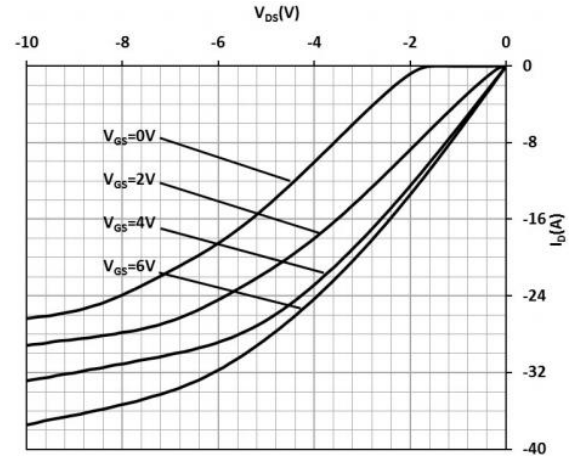
$I_D = f(V_{DS},V_{GS})$; T_j= 25 °C

Figure 6 Typ. channel reverse characteristics



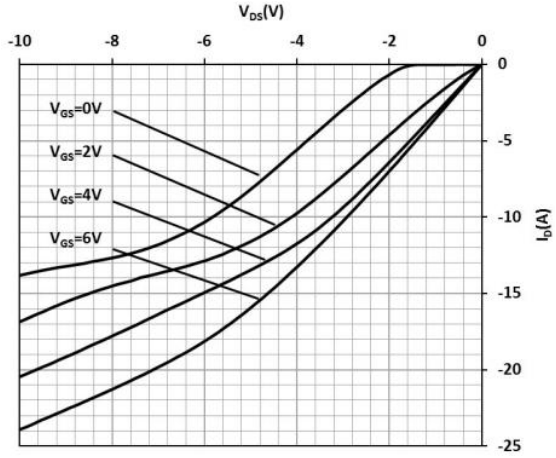
$I_D = f(V_{DS},V_{GS})$; T_j = 125 °C

Figure 7 Typ. channel reverse characteristics



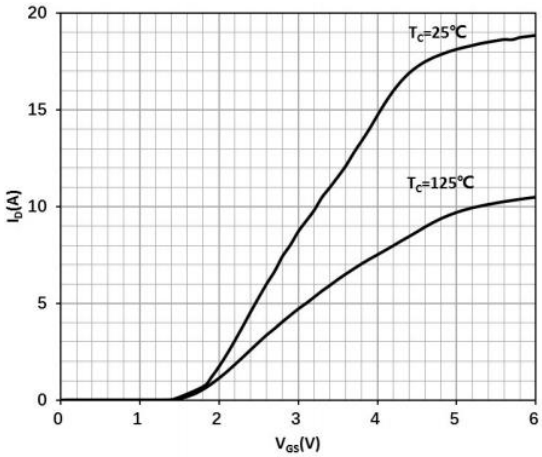
$I_D = f(V_{DS},V_{GS})$; T_j = 25 °C

Figure 8 Typ. channel reverse characteristics



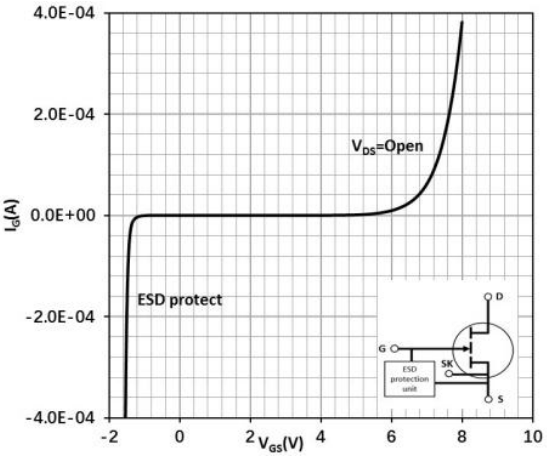
$I_D = f(V_{DS},V_{GS})$; T_j = 125 °C

Figure 9 Typ. transfer characteristics



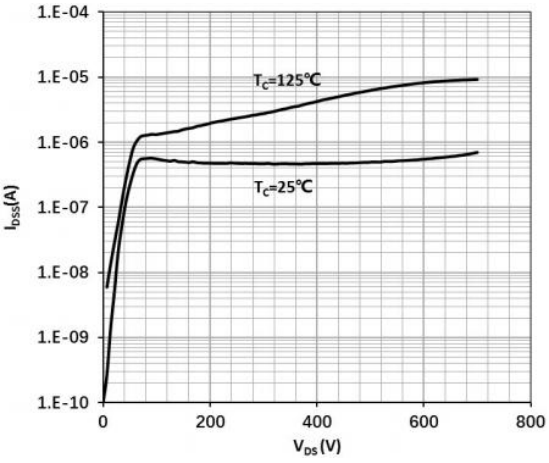
$I_D = f(V_{GS})$; V_{DS}= 3 V

Figure 10 Typ. Gate-to-Source leakage



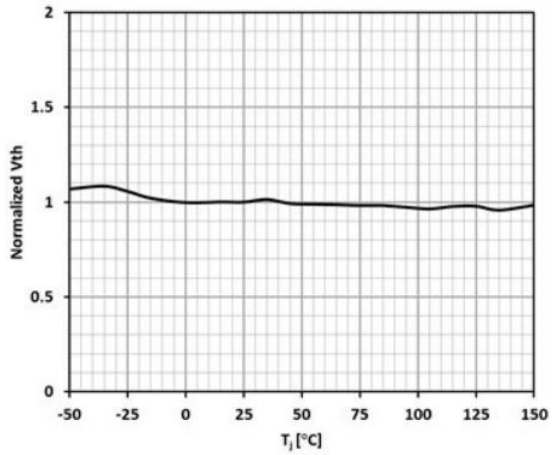
$I_G = f(V_{GS})$; I_G reverse turn on by ESD unit

Figure 11 Drain-source leakage characteristics



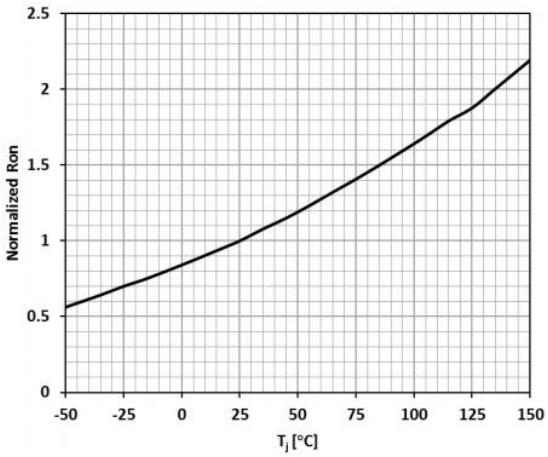
$I_{DSS} = f(V_{DS})$; V_{GS} = 0 V

Figure 12 Gate threshold voltage



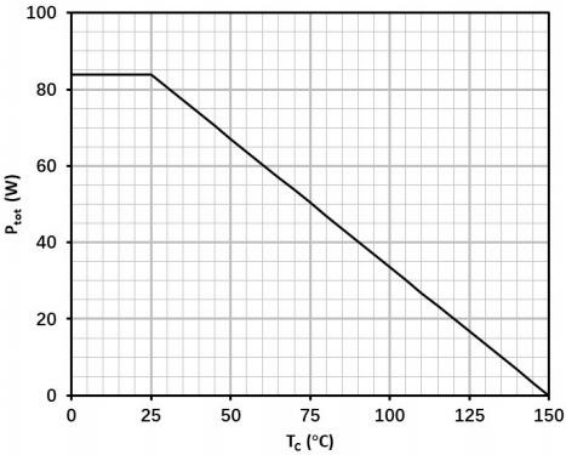
$V_{TH} = f(T_j)$; $V_{GS} = V_{DS}$; $I_D = 12.2$ mA

Figure 13 Drain-source on-state resistance



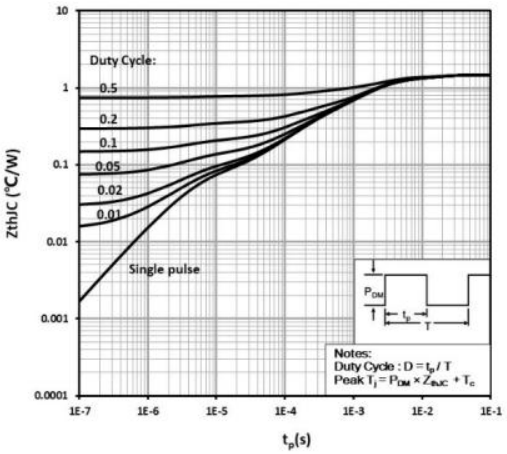
$R_{DS(on)} = f(T_j)$; $I_D = 3.9$ A; V_G=6V

Figure 14 Power dissipation



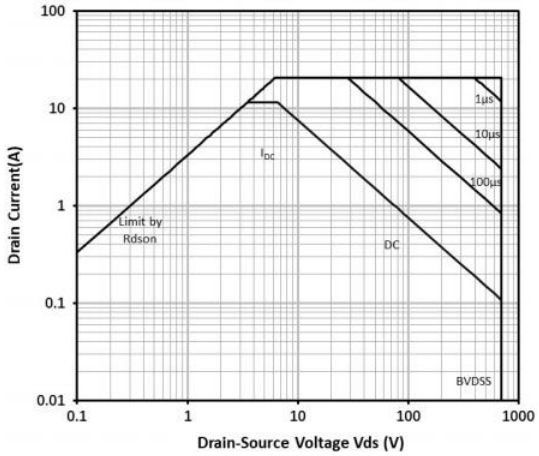
$P_{tot} = f(T_C)$

Figure 15 Max.transient thermal impedance



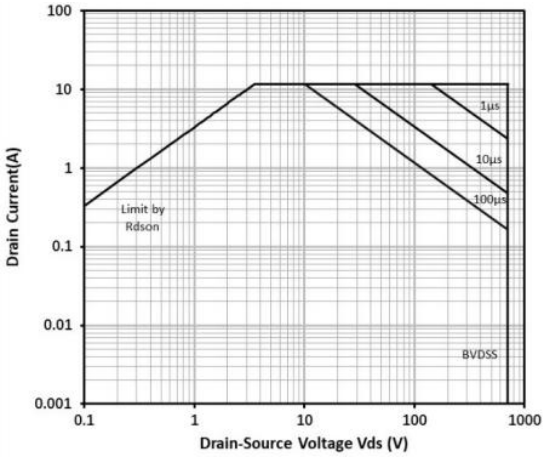
$Z_{thJC} = f(t_P, D)$

Figure 16 Safe operating area



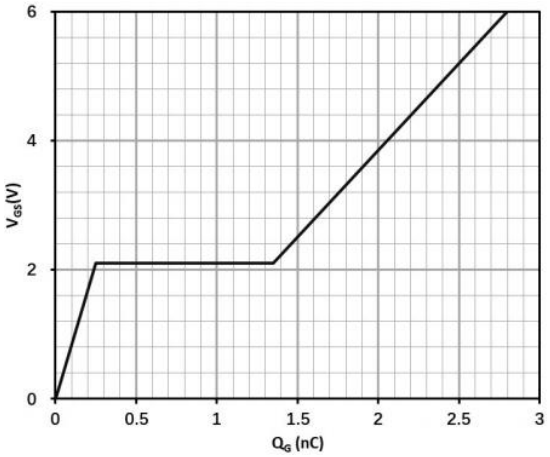
$I_D = f(V_{DS})$; $T_C = 25$ °C

Figure 17 Safe operating area



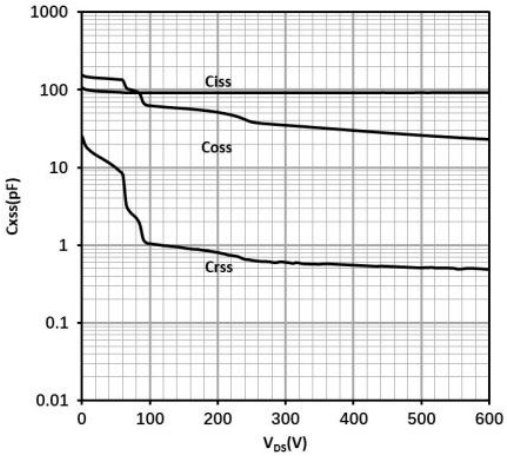
$I_D = f(V_{DS})$; $T_C = 125$ °C

Figure 18 Typ. gate charge



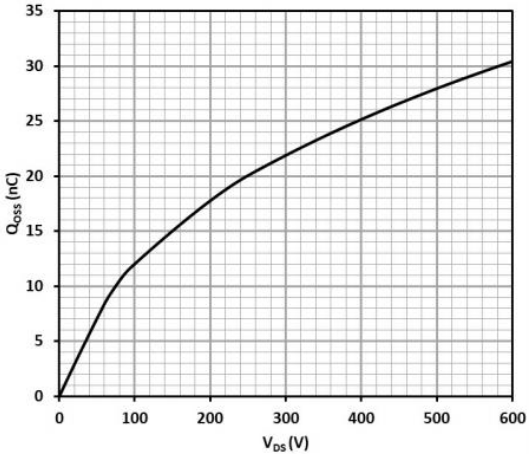
V_{GS} = f(Q_G); V_{DCLINK} = 400 V; I_D = 3.9 A

Figure 19 Typ. capacitances



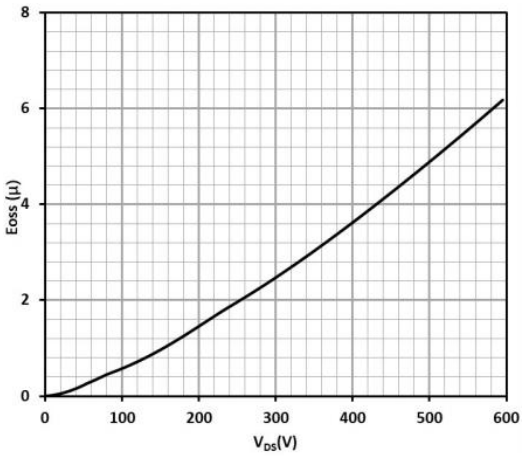
C_{XSS} = f(V_{DS}); Freq. = 100 kHz

Figure 20 Typ. output charge



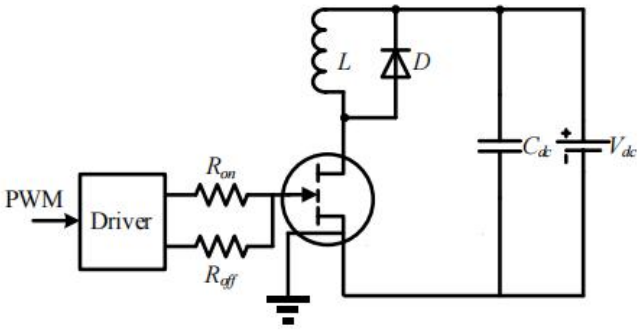
Q_{OSS} = f(V_{DS}); Freq. = 100 kHz

Figure 21 Typ. C_{OSS} stored Energy



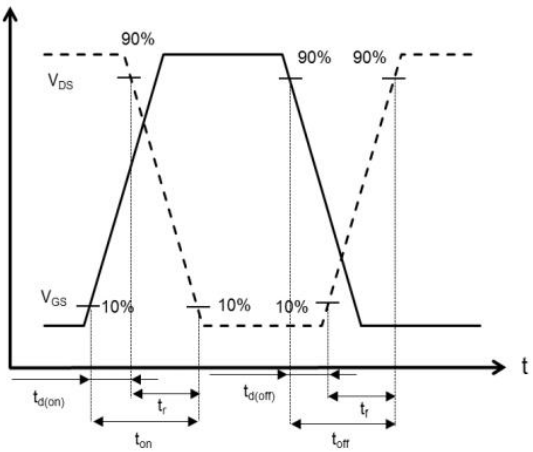
E_{OSS} = f(V_{DS}); Freq. = 100 kHz

Figure 22 Typ.Switching times with inductive load



V_{DS}=400V, I_D=8A, L=318uH, V_{GS}=6V,
R_{on}=10Ω,R_{off}=2Ω

Figure 23 Typ.Switching times waveform

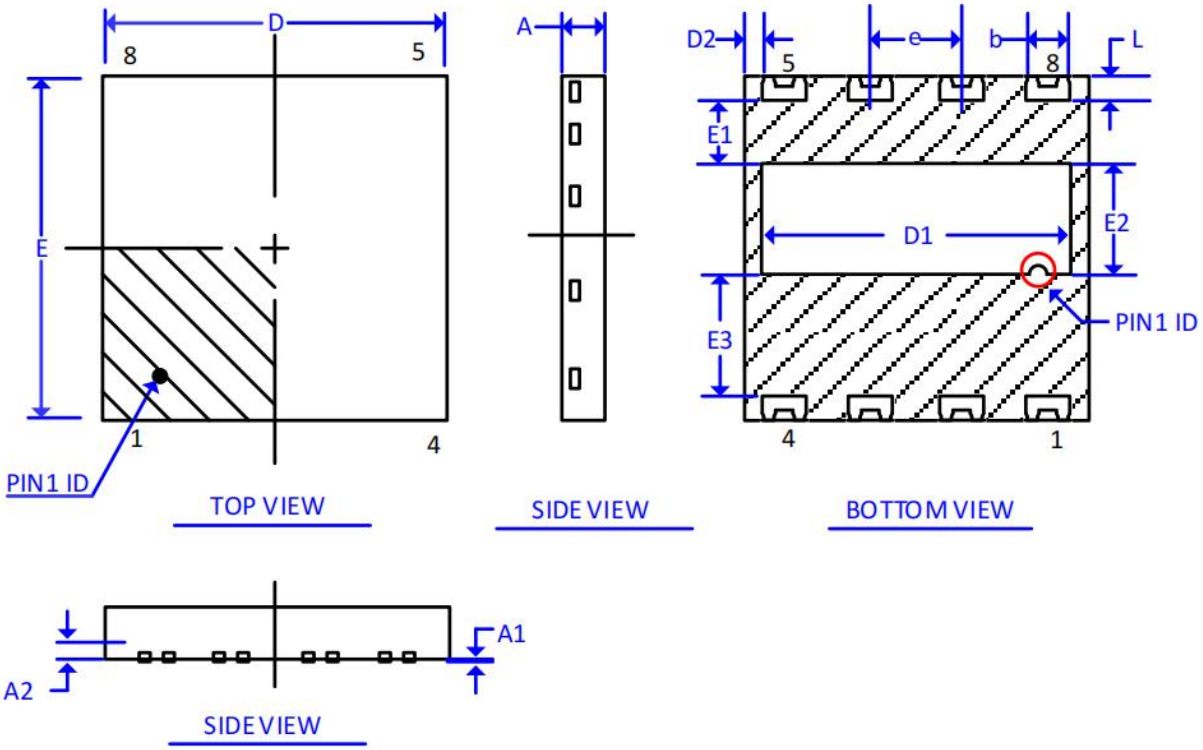


10.Package outlines

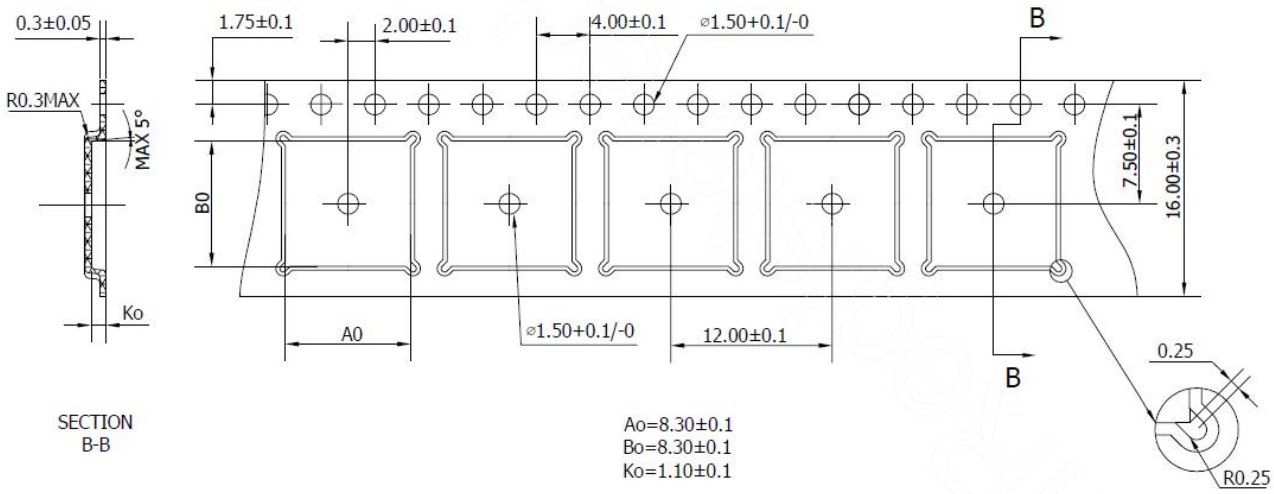
DFN8*8-8L Package Dimensions

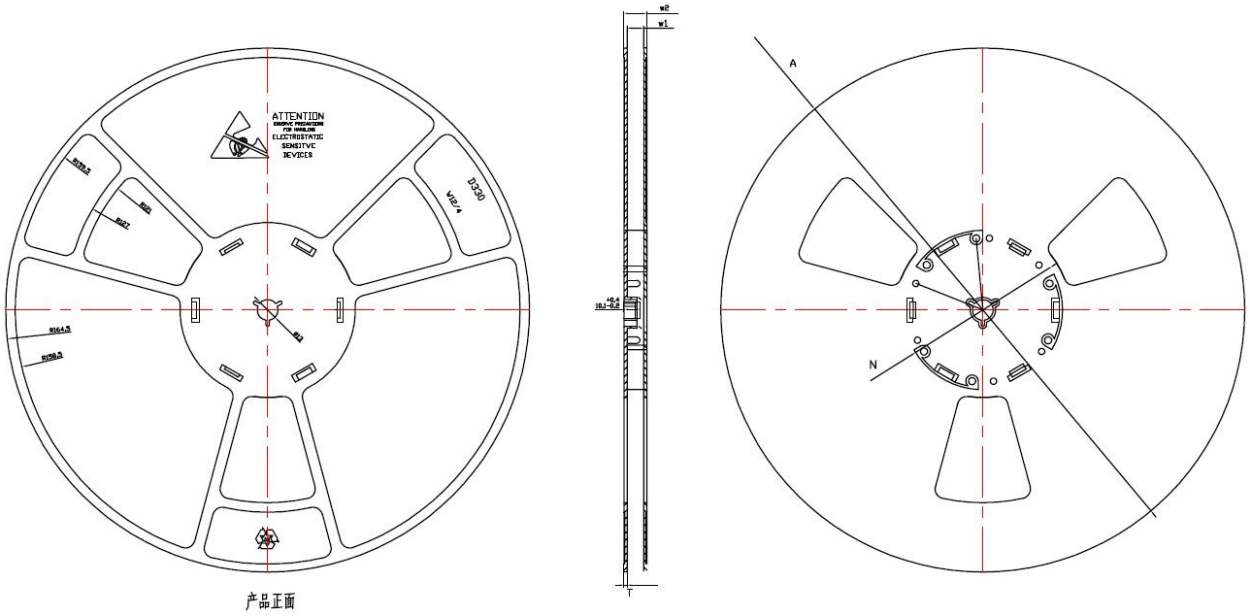
UNIT：mm

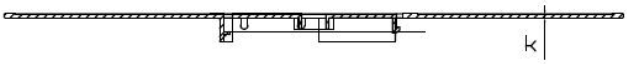
symbol	min	nom	max	symbol	min	nom	max
A	0.80	0.90	1.00	E		8.00B.S.C	
A1	0.00	0.02	0.05	E1	0.90	1.00	1.10
A2	--	0.203ref	--	E2	3.10	3.20	3.30
b	0.92	1.00	1.05	E3	2.70	2.80	2.90
D		8.00B.S.C		e		2.00B.S.C	
D1	6.84	6.94	7.04	L	0.40	0.50	0.60
D2	0.40	0.50	0.60				

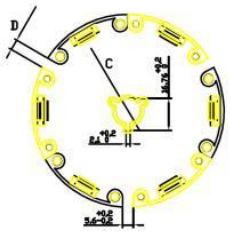


11.Reel Information









symbol	min	nom	max
A	328	330	332
N	98	100	102
C	12.90	13.10	13.30
D	5.10	5.60	6.10
w1	16.40	16.40	18.40
w2	20.60	20.60	22.60
T	1.95	2.10	2.25
K	1.30	1.40	1.55

Important Notice

版本履历表：

序号	版本号	修改时间	修改记录
1	V1.0	2023-3-21	首次发行